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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BENGHUZZI, MOHSIN M	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 10/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/630,317	ADKISSON, RICHARD W.
	Examiner	Art Unit
	Mohsin (Ben) Benghuzzi M.B.	2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *July 30, 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Hassoun et al. (US Pub 2001/0033630).

1) Regarding claim 1:

Hassoun et al. discloses a system for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$, comprising:

a phase detector operable to detect a phase between said first clock signal and said second clock signal (Paragraph 30 Line 5);

a skew state detector disposed in communication with said phase detector for generating a skew state signal which tracks a phase relationship between said first clock signal and said second clock signal (Paragraph 37 Lines 1-14, wherein, the

decremented/incremented output signal of the counter is interpreted as the skew state signal); and

a synchronizer control signal generator, responsive to said skew state signal, operating to generate at least one control signal to compensate for said skew between said first clock signal and said second clock signal (Paragraph 37 Lines 1-14, wherein, embodiment with up/down counter used is considered, and therefore, the synchronizer control signal generator is responsive to the decremented/incremented output signal of counter).

2) Regarding claim 2:

Hassoun et al. discloses the system as recited in claim 1, wherein said skew state signal is operable to compensate for greater than one clock period difference between said first clock signal and said second clock signal (Paragraph 42 Lines 2-6, wherein, 'a multiple of period' delay is interpreted as a clock period difference greater than one).

3) Regarding claim 3:

Hassoun et al. discloses the system as recited in claim 1, wherein said skew state signal is operable to track said phase relationship between said first clock signal and said second clock signal based on the location of coincident edges of said first and second clock signals (Paragraph 10 Lines 1-15 and Paragraph 11 Lines 1-5).

4) Regarding claim 4:

Hassoun et al. discloses the system as recited in claim 3, wherein said coincident edges comprise coincident rising edges (Paragraph 10 Lines 1-15).

5) Regarding claim 5:

Hassoun et al. discloses the system as recited in claim 3, wherein said coincident edges comprise coincident falling edges (Paragraph 2 Lines 9-12 and Paragraph 10 Lines 1-15).

6) Regarding claim 6:

Hassoun et al. discloses the system as recited in claim 1, wherein said skew state detector generates said skew state signal (skew_state) in response to sampled clock signals (pd_b_cr and pd_b_cf) provided by said phase detector (Paragraph 37 Lines 1-14, wherein, the decremented/incremented output signal of the counter is interpreted as the skew state signal).

7) Regarding claim 7:

Hassoun et al. discloses the system as recited in claim 1, wherein said at least one synchronizer control signal is transmitted to synchronizer circuitry (Paragraph 37 Lines 1-7, Paragraph 57 Lines 1-5, and Paragraph 43 Lines 4-11, wherein, output generator is interpreted as the synchronizer circuitry).

8) Regarding claim 8:

Hassoun et al. discloses the system as recited in claim 1, wherein said at least one synchronizer control signal is selected from the signal group consisting of c0_sel, c1_sel, core_sel, b2c_valid, c2b_valid, and c2b_valid_m (Paragraph 48 Lines 1-20).

9) Regarding claim 9:

Hassoun et al. teaches a method for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$, comprising:

determining the position of coincident edges of said first clock signal and said second clock signal (Paragraph 10 Lines 1-15);

determining if a state transition is necessary based on tracking the position of said coincident edges of said first and second clock signals (Paragraph 11 Lines 5-11 and Paragraph 37 Lines 7-14, wherein, 'determine whether to increase or decrease propagation delay', i.e., decrement/increment counter, is interpreted as determining if a state transition is necessary); and

generating a control signal indicative of said state transition, thereby compensating for said skew between said first clock signal and said second clock signal (Paragraph 37 Lines 7-14, wherein, decrement/increment output of the counter is interpreted as the control signal).

10)Regarding claim 10:

Hassoun et al. teaches the method as recited in claim 9, wherein the operation of determining the position of coincident edges comprises determining said

first clock signal and said second clock signal to be at least one quarter cycle apart (Paragraph 35 Lines 5-14, wherein, the phase shift of one-fourth of clock period is interpreted as the at least one quarter cycle apart).

11)Regarding claim 11:

Hassoun et al. teaches the method as recited in claim 9, wherein said state transition comprises a transition that tracks a negative skew difference between said first and second clock signals (Paragraph 10 Lines 1-15, wherein, 'skewed clock signal S_CLK is said to "lag" reference clock signal REF_CLK', i.e., reference clock signal REF_CLK leads skewed clock signal S_CLK is interpreted as negative skew difference).

12)Regarding claim 12:

Hassoun et al. teaches the method as recited in claim 9, wherein said state transition comprises a transition that tracks a positive skew difference between said first and second clock signals (Paragraph 10 Lines 1-15, wherein, 'reference clock signal REF_CLK is said to "lag" skewed clock signal S_CLK' is interpreted as positive skew difference).

13)Regarding claim 13:

Hassoun et al. teaches the method as recited in claim 9, wherein said control signal is operable to indicate that no skew state transition is necessary (Paragraph 11 Lines 16-18, wherein, synchronization establishment is interpreted to indicate no skew state transition is necessary).

14)Regarding claim 14:

Hassoun et al. teaches the method as recited in claim 9, wherein said control signal is indicative of a temporal relationship between said coincident edges and said second clock signal (Paragraph 57 Lines 1-5 and Paragraph 10 Lines 1-5, wherein, determination of time between rising edges is interpreted as the temporal relationship).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hassoun et al. (US Pub 2001/0033630) in view of Culley et al. (US 6,182,236).

1) Regarding claim 15:

Hassoun et al. discloses:

means for determining the position of coincident edges of said first clock signal and said second clock signal (Paragraph 10 Lines 1-15);

means for determining if a state transition is necessary based on tracking the position of said coincident edges of said first and second clock signals (Paragraph 11 Lines 5-11 and Paragraph 37 Lines 7-14, wherein, 'determine whether to increase or decrease propagation delay', i.e., decrement/increment counter, is interpreted as determining if a state transition is necessary); and

means for generating a control signal indicative of said state transition, thereby compensating for said skew between said first clock signal and said second clock signal (Paragraph 37 Lines 7-14, wherein, decrement/increment output of the counter is interpreted as the control signal).

Hassoun et al. does not disclose a computer system having an apparatus for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$. However, Culley et al. discloses a computer system having an apparatus for compensating for skew in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, where $N/M \geq 1$ (Column 4 Lines 43-53).

It is desirable to have a computer system with an apparatus for compensating for skew. This allows the clocking signal arriving at the various computer subsystems to be synchronized, and therefore, allow for accurate and proper communication of data within the computer system (See Culley et al., Column 4 Line 65 to Column 5 Line 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to have the computer system of Culley et al. include Hassoun et al.'s apparatus for compensating for skew, in order to allow the clocking signal arriving at the various computer subsystems to be synchronized, and therefore, allow for accurate and proper communication of data within the computer system.

2) Regarding claim 16:

Hassoun et al. further discloses, wherein said means for determining the position of coincident edges further comprises means for determining said first clock signal and said second clock signal to be at least one quarter cycle apart (Paragraph 35 Lines 5-14, wherein, the phase shift of one-fourth of clock period is interpreted as the at least one quarter cycle apart).

3) Regarding claim 17:

Hassoun et al. further discloses, wherein said state transition comprises a transition that tracks a negative skew difference between said first and second clock signals (Paragraph 10 Lines 1-15, wherein, 'skewed clock signal S_CLK is said to "lag" reference clock signal REF_CLK', i.e., reference clock signal REF_CLK leads skewed clock signal S_CLK is interpreted as negative skew difference).

4) Regarding claim 18:

Hassoun et al. further discloses, wherein said state transition comprises a transition that tracks a positive skew difference between said first and second clock signals (Paragraph 10 Lines 1-15, wherein, 'reference clock signal REF_CLK is said to "lag" skewed clock signal S_CLK' is interpreted as positive skew difference).

5) Regarding claim 19:

Hassoun et al. further discloses, wherein said control signal is operable to indicate that no skew state transition is necessary (Paragraph 11 Lines 16-18, wherein, synchronization establishment is interpreted to indicate no skew state transition is necessary).

6) Regarding claim 20:

Hassoun et al. further discloses, wherein said control signal is indicative of a temporal relationship between said coincident edges and said second clock signal (Paragraph 57 Lines 1-5 and Paragraph 10 Lines 1-5, wherein, determination of time between rising edges is interpreted as the temporal relationship).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lundberg et al. (US 5,811,998) discloses a state machine phase lock loop that synchronizes a first signal to a second signal, wherein, the first signal has greater frequency than the second signal.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsin (Ben) Benghuzzi whose telephone number is (571) 270-1075. The examiner can normally be reached Monday through Friday, 8:30am- 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mohsin (Ben) Benghuzzi

October 6, 2006

JAY K. PATEL
SUPERVISORY PATENT EXAMINER